complexity. This is especially of concern for Bi-CMOS processes used to manufacture bipolar and field effect devoices at the same time on the same substrate. Accordingly, a need exists for improved bipolar transistors and methods for manufacturing the same: (i) that are adapted to being "tuned" to suit particular applications, (ii) that accommodate a wide range of design space with little or no compromise of other properties, and (iii) that can be accomplished by layout adjustments without adding or significantly modifying process steps that would increase manufacturing cost. With the embodiments described below, bipolar device properties can be substantially modified just by layout adjustments. These embodiments can provide a wide design space without adding process cost. Thus, doping and masking steps can be shared with other devices on the wafer or chip without the bipolar transistors imposing undesirable constraints on process optimization.

[0016] It has been discovered that broadly tunable high gain, high breakdown voltage, bipolar transistors with significant high-side capability can be provided by incorporating multiple emitter-base junctions having different emitter-base junction depths, desirably combined with a depletable collector structure. In preferred embodiments different base doping is provided under the various emitter-base junctions. Additional tuning of the device properties can be achieved by varying the emitter-collector lateral separation.

[0017] FIGS. **1-4** show simplified cross-sectional views laterally from centerline **19** of improved bipolar transistors **20-1**, **20-2**, **20-3**, **20-4**, (collectively transistors **20**) according various embodiments of the present invention, and FIG. **5** shows, by way of example, transistor **20-1** of FIG. **1** with both halves of the transistor about centerline **19** included. The drawings illustrate the conductivity types appropriate for NPN transistors, but those of skill in the art will understand that this is merely for convenience of description and not intended to be limiting. Also for convenience of description and not intended to be limiting, the convention is adopted of referring to the various embodiments depicted in FIGS. **1-5** and various regions in such embodiments, by using a primary reference number to identify a particular element that may be present in all of the embodiments followed by a suffix to identify the particular embodiment to which it applies. For example, in the embodiment of FIG. **1**, transistor **20** is identified as transistor **20-1** and in the embodiment of FIG. **2** transistor **20** is identified as transistor **20-2**. Correspondingly, the collector buried layer (BL) is identified as BL **30-1** in transistor **20-1** of FIG. **1** and BL **30-2** in transistor **30-2** of FIG. **2**. Where it is intended to point out that a particular element may be different in various embodiments, a suffix is used and where a particular element may be substantially similar in various embodiments, no suffix is used or the same suffix may be used in multiple embodiments for those elements that can be substantially similar in such embodiments. This convention is generally followed throughout and is intended for convenience of explanation and not limitation; in particular, it is not intended to infer that elements with no suffixes or with common suffixes must be unchanged from embodiment to embodiment or similar in all such embodiments.

[0018] Referring now to FIGS. **1-5**, transistors **20** comprise substrate layer **21** having lower or bottom surface **22**. Substrate layer **21** may be a semiconductor (SC) or dielectric substrate. In a preferred embodiment for NPN transistors, substrate layer **21** is N type but may be of other conductivity type in other embodiments for either NPN or PNP transistors or may be an insulating substrate. In a preferred embodiment substrate layer **21** is a semiconductor (SC) and buried oxide (BOX) layer **24** overlies substrate layer **21**. Above BOX layer **24** is semiconductor (SC) layer **28**, preferably an epitaxial (EPI) layer extending to upper surface **23**. For convenience of description and not intended to be limiting, layer **28** is henceforth referred to as "EPI layer **28**" or "EPI **28**", but persons of skill in the art will understand that SC layer **28** formed by other means may also be used and the designation "EPI" as used herein for layer **28** is intended to include such other means of formation. Reference number **29** in FIGS. **1-5** and **8-14** is intended to refer to the combination of substrate layer **21** and layer **28**, with or without BOX layer **24** and/or buried layer **30**, as illustrated further in connection with FIGS. **7-8**. For convenience of description the terms "substrate **29**" and "substrate (**29**)" are used when referring to this combination. As is explained in more detail in connection with FIGS. **6-14**, layer **28** is desirably formed from two stacked EPI layers, EPI-1 layer **25** and EPI-2 layer **26** that join at interface **27**, but a single SC layer may also be used in other embodiments.

[0019] Lying within EPI layer **28** at or near interface **27** is (e.g., N type) buried layer (BL) **30** of lateral width **31**. Extending from (e.g., N type) BL **30** substantially to surface **23** is (e.g., N type) WELL region **34**. Collector contact (e.g., N+) **35** is provided at surface **23** in WELL region **34**, and is coupled to collector terminal **92**. Extending into EPI layer **28** from surface **23** is (e.g., N type) first emitter region **40**. Emitter contact (e.g., N+) **41** is provided at surface **23** in Ohmic contact with (e.g., N type) first emitter region **40** and is coupled to emitter terminal **90**. Also extending into EPI layer **28** from surface **23** are shallow trench isolation (STI) regions **55** of, for example, a dielectric such as silicon oxide. Toward the right in FIGS. **1-4** and at both left and right in FIG. **5**, are (e.g., dielectric) deep trench isolation (DTI) regions **60**, also typically of silicon oxide, extending in preferred embodiments substantially from surface **23** to substrate layer **21**. In combination with BOX layer **24**, DTI regions **60** serve to isolate transistors **20** from other devices or regions on substrate layer **21**. In a preferred embodiment, conductive (e.g. poly-semiconductor) core **61** is provided in DTI regions **60** but may be omitted in other embodiments. Techniques for creating such STI and DTI regions are well known in the art. STI regions **55** are particularly identified as STI regions **55-11**, **55-12**, **55-13** in transistor **20-1** of FIGS. **1** and **5**, and as STI regions **55-21**, **55-22**, **55-23** in transistors **20-2**, **20-3**, **20-4** of FIGS. **2-4**.

[0020] Underlying surface **23** at the left of STI regions **55-11** and **55-21** are (e.g., N type) first emitter regions **40** with (e.g., N+) of depth **46** from surface **23** and with emitter contacts **41** at surface **23**. Underlying STI regions **55-11** and **55-21** are (e.g., N type) second emitter regions **43** of lateral width **44**, particularly identified as (e.g., N type) second emitter regions **43-1** of width **44-1** in FIGS. **1** and **5** and (e.g., N type) second emitter regions **43-2** of width **44-2** in FIGS. **2-4**, and collectively referred to as second emitter regions **43**. Underlying (e.g., N type) first emitter regions **40** are (e.g., P type) first base regions **50** that form (e.g., NP) first emitter-base junctions **45** at depth **46** from surface **23**. Underlying (e.g., N type) second emitter regions **43** are (e.g., P type) second base regions **51** that form (e.g., NP) second emitter-base junctions **47** at depth **48** from surface **23**. It will be understood by those of skill in the art that junctions **45** and **47** may be NP or PN junctions depending upon whether NPN or